Hewlett-Packard Company
PDNO 200209237-1
Inventor: Anthony
HP Contact # (650)236-4890

A MAGNETIC MEMORY CELL HAVING A SOFT REFERENCE LAYER

RELATED APPLICATIONS

This patent is a continuation-in-part of, and claims priority to, the co-pending U.S. patent application bearing serial no. 10/351,013, filed 1-25-03 now Patent No. 6,891,745 which is a divisional application of a U.S. patent application bearing serial no. 09/963,171 now issued as U.S. Pat. No. 6,576,969 B2.

BACKGROUND

A memory chip generally comprises a plurality of memory cells that are deposited onto a silicon wafer and addressable via an array of column conducting leads (bit lines) and row conducting leads (word lines). Typically, a memory cell is situated at the intersection of a bit line and a word line. The memory cells are controlled by specialized circuits that perform functions such as identifying rows and columns from which data are read from or to which data are written. Typically, each memory cell stores data in the form of a "1" or a "0," representing a bit of data.

An array of magnetic memory cells can be referred to as a magnetic random access memory or MRAM. MRAM is generally nonvolatile memory (i.e., a solid state chip that retains data when power is turned off). At least one type of magnetic memory cell includes a data layer and a reference layer, separated from each other by at least one intermediate layer. The data layer may also be referred to as a bit layer, a storage layer, or a sense layer. In a magnetic memory cell, a bit of data (e.g., a "1" or "0") may be stored by "writing" into the data layer via one or more conducting leads (e.g., a bit line and a word line). A typical data layer might be made of one or more ferromagnetic materials. The write operation is typically accomplished via one or more write currents that set the orientation of the magnetic moment in the data layer